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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,996	11/17/2003	Shinichi Shuto	XA-9974	9398

181 7590 12/14/2006

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,996	SHUTO ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-18,22 and 23* is/are allowed.

6)☒ Claim(s) *1-4,10-13 and 19-21* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 10, 11, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadderman, U.S. Patent No. 5,805,473, in view of Evoy, U.S. Patent No. 6,062,480[1].

Regarding claim 1, Hadderman teaches a semiconductor processing system [Fig. 1, PCMCIA card] comprising an interface control circuit and a processing circuit, and attached to an external apparatus so as to receive an operation power supply therefrom, configured to detect a loss of voltage, at which time the card causes a processing circuit to end processing upon detection that a power supply is disconnected [col. 7, lines 7-10, Fig. 4, step 405].

Hadderman does not teach a first external terminal to detect a potential change when it is disconnected from the external apparatus.

Evoy teaches a PCMCIA card with card detect pins [first external terminal] that are shorter than power pins [second external terminal], such that upon removal of the card, the card

detect pins sense the removal before power is removed from the card via the power pins [col. 2, lines 49-53, col. 4, lines 60-64].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Hadderman and Evoy by implementing the card detect pins of Evoy in the system of Hadderman. Both Hadderman and Evoy are directed towards PCMCIA cards that detect accidental removal. Additionally, Evoy teaches that the use of card detect pins for PCMCIA is part of the conventional implementation ["Background of the Invention"]. Although Hadderman teaches the detection of card removal, Hadderman is silent as to the method of such detection. The teachings of Evoy would improve Hadderman by providing this missing element.

Regarding claim 3, the combination of Hadderman and Evoy teaches the limitations of claim 1, and also teaches the starting up on a power supply circuit to supplement the operation power supply of the processing circuit [Fig. 1, independent power source 115, Fig. 4, step 415].

Regarding claim 4, Evoy teaches that the card detect pins [first external terminal] are monitored for a potential change when they are disconnected from the external device [col. 2, lines 49-53].

Regarding claim 10, Hadderman teaches said processing circuit includes a non-volatile memory enabling information to be written/erased therein/therefrom electrically; and wherein said interface control circuit is a control circuit for controlling both of said external interface and said non-volatile memory [Hadderman, Fig. 1, DRAM[2]].

Regarding claim 11, Hadderman teaches that ending processing adjusts threshold voltages of non-volatile memory cells so as to be set in a predetermined threshold voltage range during an erasure/write processing [Fig. 4, step 410].

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[1] Evoy and Hadderman both cited in prior office action.
[2] Although DRAM is normally considered volatile, in this case the DRAM of Hadderman is equipped with a data-retention mode, so it may be considered non-volatile.

Regarding claims 19 and 21, Evoy teaches that the card detect pins and power pins have different lengths.

Claims 2 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of Konishi et al., U.S. Patent No. 5,745,912[3].

Regarding claim 2, Evoy teaches:

a semiconductor processing system comprising an interface control circuit and a processing circuit, and attached to an external apparatus so as to receive an operation power supply therefrom, wherein said interface control circuit, when said system is removed from the external apparatus, detects a potential change that occurs at a first external terminal of said system which is disconnected from a predetermined terminal of the external apparatus before the power supply from the external apparatus is disconnected from a second external terminal of the system [see rejection of claim 1].

Evoy does not teach the storing of a flag denoting an occurrence of a power supply shutoff.

Konishi teaches a memory card apparatus that stores a flag that denotes occurrence of a power supply shutoff [col. 4, lines 43-59].

It would have been obvious to one of ordinary skill in the art to combine the features of Evoy with Konishi by adding a flag that indicates a loss of power to Evoy, such as that taught by Konishi. Both Evoy and Konishi are directed towards removable peripheral card devices, and as such may be considered to be analogous subject matter. Additionally, Konishi addresses the scenario that is presented by Evoy – namely, removal of the peripheral card device that results in a loss of power supplied to the device. The addition of Konishi's teachings would improve

[3] Cited in prior office action.

Evoy by adding a means for detecting when an error has been introduced during a memory read/write operation by a sudden loss of power or removal of the device from an external apparatus [col. 3, lines 35-45].

Regarding claim20, Evoy teaches that the card detect pins and power pins have different lengths.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadderman in view of Evoy as applied to claim 10 above, and further in view of Konishi.

Regarding claim 12, Evoy/Hadderman does not teach the setting of a flag. Konishi teaches the setting of a flag in a location in link table that is associated with a particular memory location during a memory write operation [col. 6, lines 3-18].

It would have been obvious to one of ordinary skill in the art to combine the features of Evoy/Hadderman with Konishi by setting a flag associated with a memory location, such as that taught by Konishi. Both Evoy/Hadderman and Konishi are directed towards removable peripheral card devices, and as such may be considered to be analogous subject matter. Additionally, Konishi addresses the scenario that is presented by Evoy/Hadderman – namely, removal of the peripheral card device that results in a loss of power supplied to the device. The addition of Konishi's teachings would improve Evoy/Hadderman by adding a means for detecting when an error has been introduced at a particular memory location during a memory read/write operation by a sudden loss of power or removal of the device from an external apparatus [col. 3, lines 35-45].

Regarding claim 13, Evoy/Hadderman/Konishi teaches that ending processing includes a completing processing for the current erasure/write processing for a non-volatile memory cell [col. 7, lines 7-10, Fig. 4, step 405].

Allowable Subject Matter

Claims 14-18, 22, and 23 are allowed.

Claims 5-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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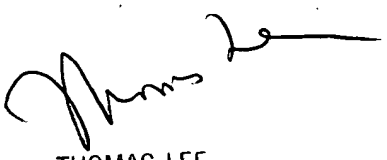

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